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Single-Stage Switched-Capacitor Module (S^3CM) Topology for Cascaded Multilevel Inverter

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Abstract: - A two-stage switched-capacitor based multilevel inverter possesses a drawback such that switches in the second stage (i.e. H-bridge) endure higher voltage stress. To resolve this problem, this letter proposes a single-stage switched-capacitor module (S^3CM) topology for cascaded multilevel inverter which ensures the peak inverse voltage across all switches within the dc source voltage. Nine voltage levels can be generated with only one dc source and two incorporated capacitors. Hence, the number of isolated dc sources are significantly reduced compared to cascaded H-bridge. In addition, voltage boosting gain of two is achieved. A comparative analysis against the recent topology reveals that the proposed S^3CM topology achieves switch count reduction. The operation of the proposed topology is validated through circuit analysis followed by experimental results of a single module (9-level) prototype.

Index Terms: Cascaded multilevel inverter, single-stage, switched-capacitor module

I. INTRODUCTION

Cascaded H-bridge (CHB) multilevel inverter (MLI) is ubiquitous in high-voltage applications due to its inherent modularity [1]. Alternatively, there are recent attempts to replace H-bridge by establishing module topologies which is capable of generating more voltage levels with reduced switch count [2].

Among the various module topologies, an envelope type of module presented in [3] utilizes a combination of T-type inverter and some additional switches to control four unequal dc sources. On the other hand, [4] demonstrated a square T-type module comprises two back-to-back connected T-type inverters which is able to produce 17 levels with only 12 switches and four unequal dc sources. Similar concept with further switch count reduction is proposed in [5], [6]. Nonetheless, unlike CHB where all switches are restricted their peak inverse voltage (PIV) within one level (one dc source), these newly established module topologies entails some of their switches to block voltage greater than one level (sum of all the dc sources) during OFF state, thus renders them less appropriate for high-voltage applications. Despite multiple series-connected switches can be implemented to cater for PIV greater than one level, they will essentially forfeit their merit of switch count reduction compared to H-bridge.

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Switched-capacitor based topology is another promising compact module which is gaining popularity in the recent years, mainly attributed to its voltage boosting capability which has made the reduction in the number of dc sources possible [7], [8]. An innovative switched-capacitor module (SCM) topology recently reported in [9] is capable of generating up to 9 voltage levels with a single dc source. Voltage boosting is validated with the achievement of its maximum voltage level twice of the input dc source. Capacitor voltage balancing is not a concern since two capacitors are integrated such that their average voltage are equal during operation.

It is worth mentioning that SCM in [9] is a two-stage topology consisting of a switched-capacitor circuit and a H-bridge, as illustrated in Fig.1. Switches in the H-bridge (second stage) have to withstand voltage twice of the input dc source. In case it is used for high-voltage applications, two series-connected switches are required for S7 – S10 and S5 to ensure the PIV of all switches do not exceed dc source voltage (V_{dc}). In this instance, each SCM is comprised of a diode and a total switch count of 15.

The initiative of this work is to establish an alternative topology, termed as single-stage switched-capacitor module (S^3CM) which resolved the drawbacks of Fig. 1, while at the same time retaining all its benefits. The PIV of all switches in the proposed S^3CM are within the dc source voltage, V_{dc}. The paper is organized as follows: section II presents the proposed module topology for cascaded MLI and the comparative analysis against Fig. 1 and CHBMLI, section III discusses the experimental results of a prototype, and finally section IV draws the conclusion.

II. PROPOSED S^3CM TOPOLOGY

The proposed S^3CM topology is able to generate up to nine voltage levels. It is constituted by twelve switches, two capacitors and only one dc source, as depicted in Fig. 2. The number of levels and output voltage can be further increased by cascading multiple (N) modules. It is worth emphasized that the PIV of all switches in the proposed S^3CM topology are equivalent to V_{dc}, with the exception of two switches, i.e. S9 and S10 which blocks only half of the V_{dc}. With merely low voltage rating switches, it can accomplish output voltage up to twice V_{dc}. On that account, it does not require series-connected switches when high-voltage applications is considered.

Detailed circuit analysis concerning switching states of the proposed module topology is illustrated in Fig. 3. A comparative

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analysis among cascaded MLI with the proposed S^{3}CM, the SCM topology [9], and the H-bridge is conducted in Fig. 4. For fair comparison, voltage stress of all the switches in these topologies are kept within V_{dc}. Therefore, two series-connected switches must be considered for S5 and S7–S10 for the SCM topology in [9] (Fig. 1).

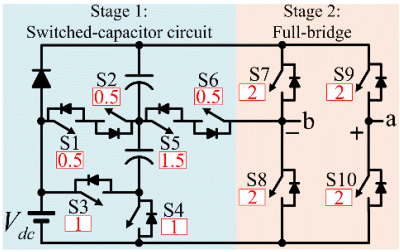

Fig. 1. Switched-capacitor module (SCM) topology presented in [9].

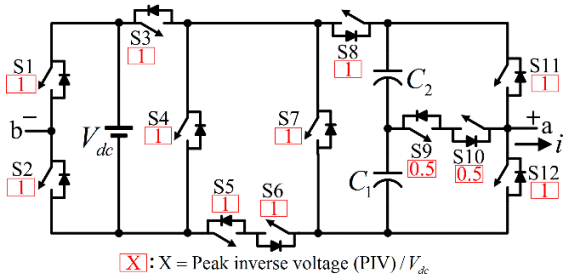

Fig. 2. The proposed single-stage switched-capacitor module (S^{3}CM) topology for cascaded MLI.

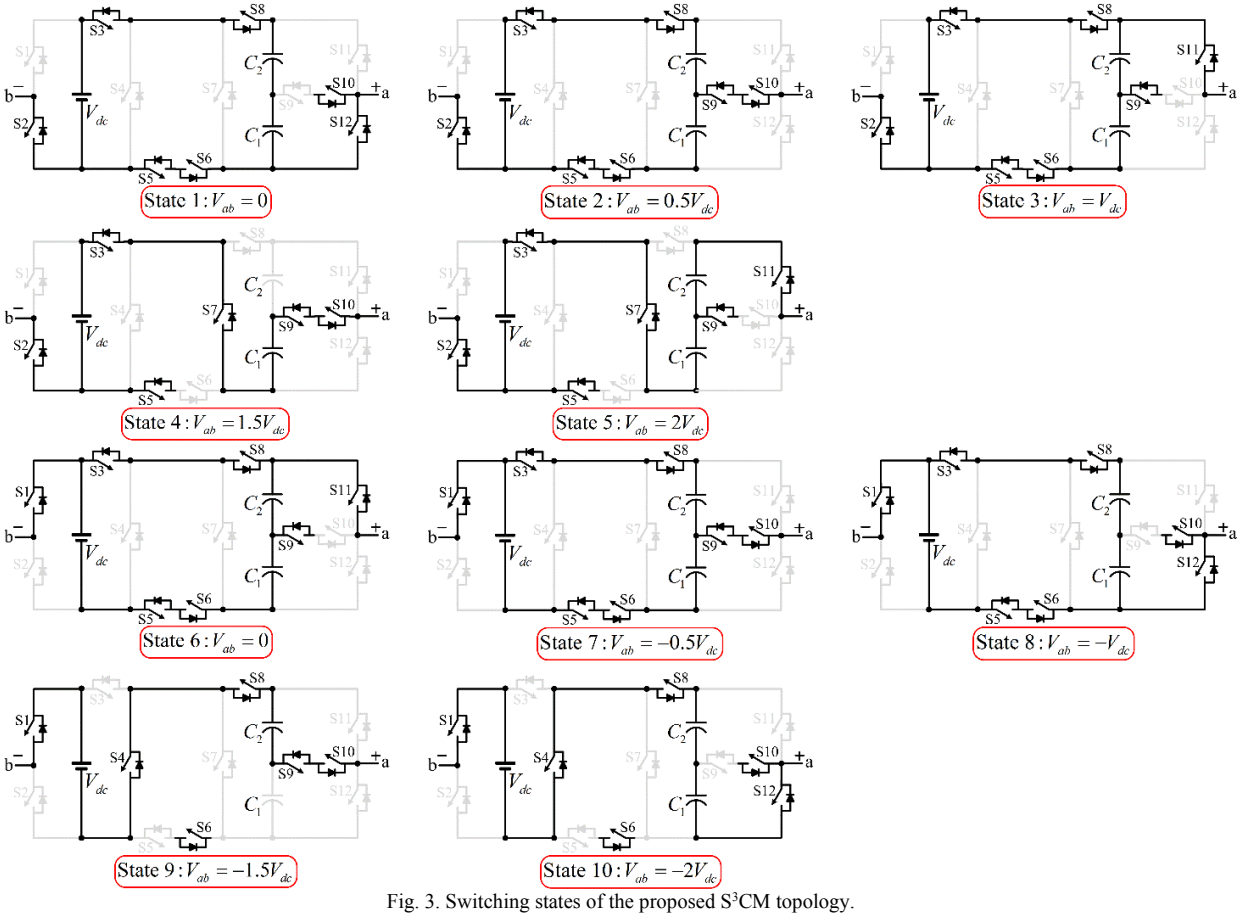

Fig. 3. Switching states of the proposed S^{3}CM topology.

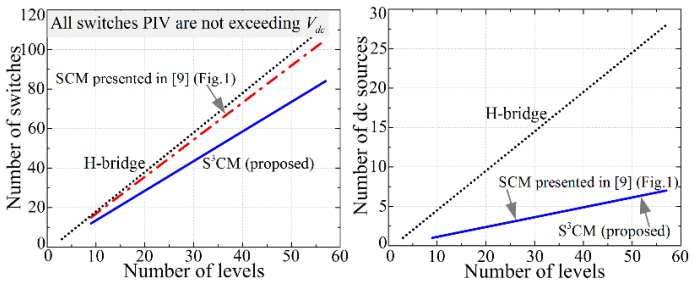

Fig. 4. Comparative analysis for cascaded MLI using the proposed S^{3}CM, SCM [9] (Fig. 1) and H-bridge.

TABLE I
EQUATIONS FOR CASCADED MLI USING DIFFERENT MODULES WITH ALL SWITCHES PIV WITHIN THE DC SOURCE, V_{dc}

	Proposed S^{3}CM	SCM in [9]	H-Bridge
Levels	8N+1	8N+1	2N+1
Switches	12N	15N	4N
Diodes	-	N	-
DC sources	N	N	N
Capacitors	2N	2N	-
Voltage gain	2	2	1

N = number of cascaded modules/H-bridges
Voltage gain = ratio of the maximum voltage level to the sum of all dc sources

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With cascaded H-bridge as a benchmark, cascaded MLI using both the SCM topology in [9] and the proposed S^{3}CM topology illustrate less number of switches for a given voltage level, with the latter results in more switch count reduction. Besides, both topologies demonstrate the same number of dc sources, which is also significantly less than the cascaded H-bridge for all voltage levels. It is also worth emphasized that cascaded H-bridge and the proposed S^{3}CM topology require no diode in their circuitry, while N diodes are mandatory in the SCM topology [9]. All equations related to the compared modules for cascaded MLI are summarized in Table I.

Some detailed comparisons between the proposed S^{3}CM topology and the SCM topology in [9] are depicted in Fig. 5. It is worth emphasize that the switching sequences of the capacitors in S^{3}CM are identical to that in [9]. C_1 discharges for a longer period during the positive half-cycle while C_2 discharges for a longer period in the negative half-cycle. Nonetheless, they have equal discharging periods when symmetrical ac voltage is under consideration. This implies their equal average voltage, as similar to [9].

The number of conducting semiconductor devices and the number of switching transitions between both topologies are also considered for power conversion efficiency comparison purpose. Considering PIV for all switches are within V_{dc}, the proposed S^{3}CM has less conducting switches for $1.5V_{dc}$, $2V_{dc}$, $-1.5V_{dc}$ and $-2V_{dc}$, indicating its lower conduction loss. Besides, it also presents less number of switch/diode commutations for all voltage level transitions, except when the transition is between V_{dc} and $1.5V_{dc}$. Its two zero states introduces more switching transitions when the output voltage is 0V. The proposed S^{3}CM topology exhibits a total of 56 switching transitions over one fundamental cycle, as oppose to a total of 88 switching transitions in the SCM topology [9], which signifies its advantage of lower switching loss.

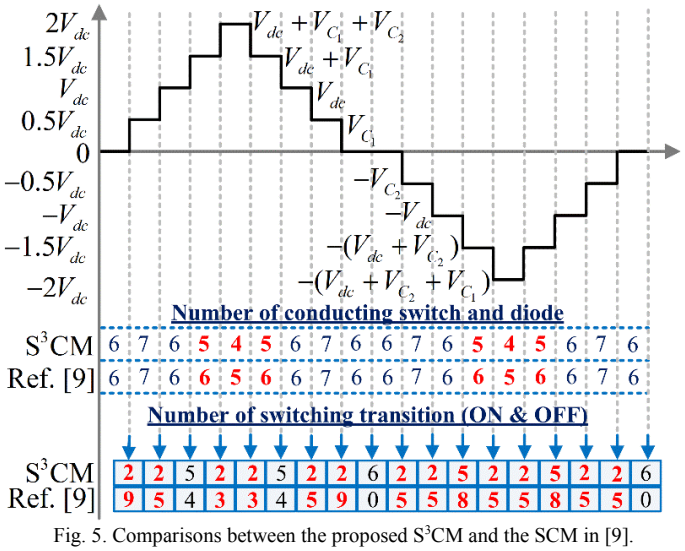

Fig. 5. Comparisons between the proposed S^{3}CM and the SCM in [9].

III. SIMULATION AND EXPERIMENTAL RESULTS

Simulations were conducted for both the steady-state and dynamic conditions. Fig. 6 shows the output voltage, load current and capacitors voltage for N=1. Seven voltage levels are clearly seen with both capacitors voltages balanced averagely about 100V. Unequal capacitances for C_1 and C_2 were then simulated considering 20% tolerances in each capacitor. Result depicted in Fig.7 demonstrates that both the capacitor voltages are still oscillating around 100V albeit the different peak-to-peak magnitude. The voltage ripple across C_1 is smaller than that across C_2 due to its higher capacitance. A step load change was also conducted with load current increased to twice its original magnitude. Findings from Fig.8 show that the capacitors voltages are slightly unbalanced after the step load change and gradually stabilizes at 100V, which once again confirming its capacitor voltage balancing ability during operation.

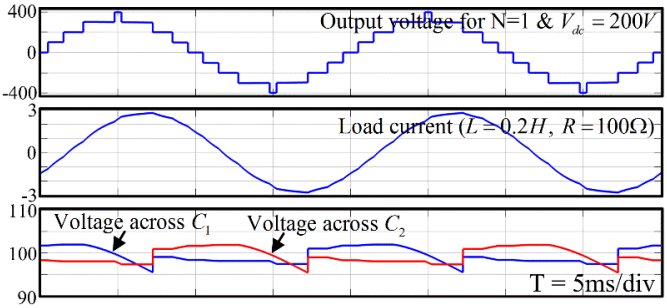

Fig. 6. Simulated steady-state waveforms for single S^{3}CM (9-level).

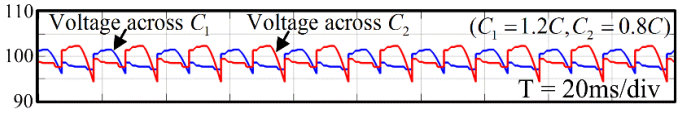

Fig. 7. Simulated capacitor voltage considering 20% tolerances in capacitance.

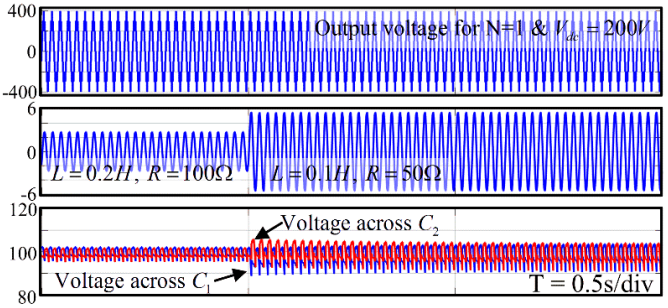

Fig. 8. Simulated waveforms for step load change.

Sinusoidal pulse width modulation (SPWM) which is prevalently used in industrial applications is employed to further verify the operation of the proposed S^{3}CM. The corresponding simulation results under two different modulation indexes for the case of purely resistive load and resistive-inductive load are shown in Fig. 9(a) and (b) respectively. Three voltage levels, i.e. $0.5V_{dc}$, 0, and $-0.5V_{dc}$ are sufficient for generating low voltage at modulation index of 0.2, indicating the feasibility of wide range modulation index in the proposed S^{3}CM topology.

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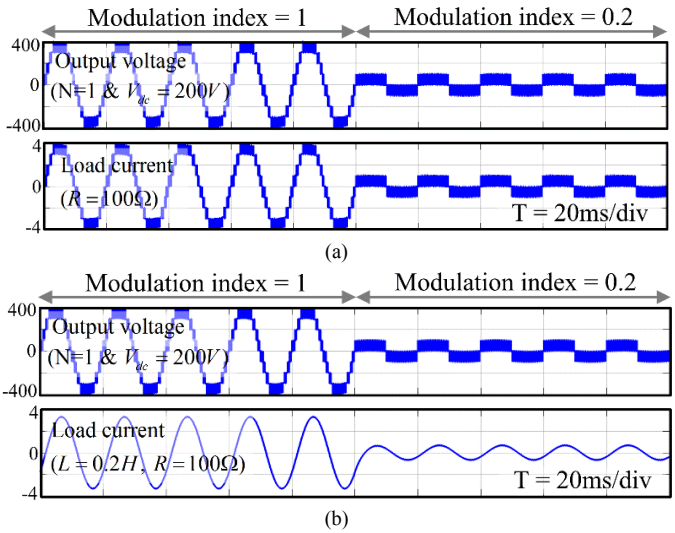

Fig. 9. Simulated waveforms with sinusoidal pulse width modulation (SPWM) for (a) purely resistive load, and (b) resistive-inductive load.

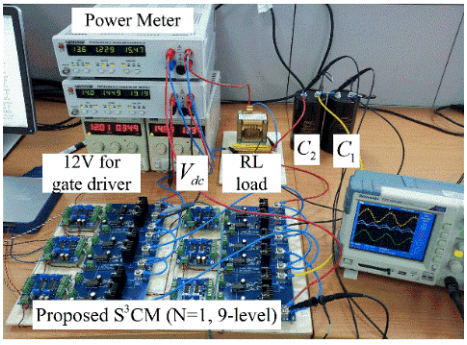

Fig. 10. Experimental prototype.

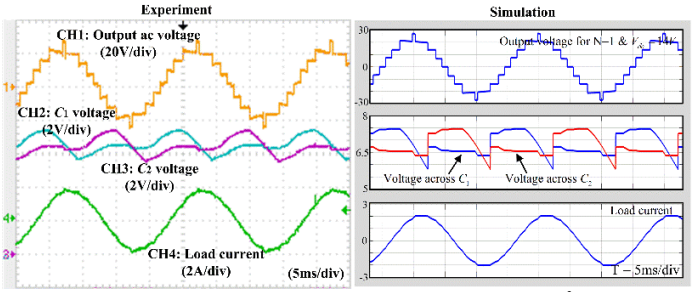

Fig. 11. Experimental and simulation waveforms of the proposed S³CM topology (N=1, 9-level) operated under resistive-inductive load.

For further verification, an experimental prototype depicted in Fig. 10 has been tested. With limited resources, 14V dc source and resistive-inductive load with power factor of 0.93 was considered. The efficiency recorded at 15.47W is 80.61%. The experiment waveforms depicted in Fig. 11 shows good agreement with the theoretical analysis, where nine voltage levels are clearly seen in the output voltage. The maximum voltage level is approximately 28V, validating the voltage boosting capability of the proposed S³CM topology. Two capacitor voltages are balanced with their average voltage approximately 7V, which is half of the dc source. Note that the simulation considers ideal capacitors (C_1 and C_2) without internal series resistance, their voltage waveforms are thus showing instant charging with approximately zero rise time, as opposed to the slower rising time as shown in the experiment. In both simulation and experimental waveforms, the longest discharging period for C_1 and C_2 takes place when the output voltage equals to $\{1.5V_{dc}, 2V_{dc}\}$ and $\{-1.5V_{dc}, -2V_{dc}\}$ respectively. Good agreement between experimental and simulation waveforms further confirms the validity of the proposed S³CM topology.

IV. CONCLUSION

In this letter, a 9-level inverter module based on single-stage switched-capacitor circuit is established for cascaded MLI. The proposed S³CM topology requires only single dc source with a voltage boosting gain of two. Circuit analysis demonstrated that the voltage stress across all switches are within the dc source voltage. Therefore, it is capable of generating more levels and higher voltages up to twice the dc source by using switches with low voltage rating. Comparative analysis against the recent SCM topology and the H-bridge for cascaded MLI validates its merits of reduced switch count as well as reduced dc source count. The performance of the proposed topology are convincingly validated via experiments, with all the results are in good agreement with theoretical analysis. The improvements of the proposed S³CM topology made it an attractive alternative for high-voltage dc-ac power conversion systems.

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